WHAT IS CLAIMED IS:

1. A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation layer on a substrate,

introducing impurities into said first insulation layer, and

embedding and forming a first conductive layer in said first insulation layer.

2. The fabrication method of a semiconductor device according to claim 1, wherein said step of forming a first conductive layer includes the step of embedding the first conductive layer in said first insulation layer so as to expose a surface of said first conductive layer, and

said fabrication method further comprising the steps of:

forming a second insulation layer on said first insulation layer,

forming a contact hole in said second insulation layer, exposing a portion of said first conductive layer, and

forming a second conductive layer in said contact hole, electrically connected to said first conductive layer.

3. The fabrication method of a semiconductor device according to claim 2, further comprising the step of introducing impurities into said second insulation layer.

4. The fabrication method of a semiconductor device according to claim 2, comprising, after formation of said second insulation layer and before formation of said contact hole, the steps of:

forming a first mask pattern on said second insulation layer,

forming a third insulation layer on said second insulation layer and on said first mask pattern,

forming a second mask pattern on said third insulation layer, having an opening larger than said first mask pattern, and

etching said third insulation layer using said second mask pattern to

form a trench in said third insulation layer reaching to said first mask pattern,

wherein said step of forming a contact hole includes the step of etching said second insulation layer using said first mask pattern, and

wherein said step of forming a second conductive layer includes the step of forming a third conductive layer in said trench, electrically connected to said second conductive layer, in addition to formation of said second conductive layer.

5. The fabrication method of a semiconductor device according to claim 4, further comprising the step of introducing impurities into said third insulation layer.

6. The fabrication method of a semiconductor device according to claim 1, further comprising the step of forming a fourth insulation layer on said substrate, prior to formation of said first insulation layer,

wherein said step of introducing impurities into the first insulation layer is carried out under a condition where introduced impurities arrive at an interface between said first insulation layer and said fourth insulation layer.

7. The fabrication method of a semiconductor device according to claim 1, wherein said first insulation layer includes a silicon oxide film containing at least 1% of carbon.

8. The fabrication method of a semiconductor device according to claim 2, wherein said second insulation layer includes a silicon oxide film containing at least 1% of carbon.

9. The fabrication method of a semiconductor device according to claim 4, wherein said third insulation layer includes a silicon oxide film containing at least 1% of carbon.

10. The fabrication method of a semiconductor device according to claim 1, wherein said first insulation layer includes an inorganic SOG film.

11. The fabrication method of a semiconductor device according to claim 2, further comprising, after formation of said second insulation layer and before formation of said contact hole, the steps of:

forming a third mask pattern on said second insulation layer,

etching said second insulation layer using said third mask pattern to selectively reduce thickness of said second insulation layer, and

forming a fourth mask pattern on said second insulation layer so as to expose a portion of the region reduced in thickness,

wherein said step of forming a contact hole includes the step of etching said second insulation layer using said fourth mask pattern, and

said step of forming a second conductive layer includes the step of forming a third conductive layer on said region reduced in thickness, electrically connected to said second conductive layer, in addition to formation of said second conductive layer.

12. The fabrication method of a semiconductor device according to claim 1, further comprising the steps of:

forming a second insulation layer on said first insulation layer,

forming a fifth mask pattern on said second insulation layer,

etching said second insulation layer using said fifth mask pattern to form a contact hole in said second insulation layer, exposing a portion of said first conductive layer,

after removing said fifth mask pattern, forming a resist film in said contact hole and on said second insulation layer,

forming a sixth mask pattern on said contact hole, having an opening larger than that contact hole, by patterning said resist film on said second insulation layer,

etching said second insulation layer using said sixth mask pattern to selectively reduce thickness of said second insulation layer,

removing the resist film remaining in said contact hole and said sixth

mask pattern, and

forming a second conductive layer in said contact hole, electrically connected to said first conductive layer.

13. The fabrication method of a semiconductor device according to claim 2, further comprising the step of introducing impurities into said second insulation layer, prior to forming said contact hole in said second insulation layer.

14. A semiconductor device comprising:

a first conductive layer having a top face on a first plane,

a first insulation layer into which impurities are introduced, having a top face on a second plane parallel to said first plane, and

a second insulation layer into which impurities are introduced, having a top face on a third plane parallel to said second plane, and

a second conductive layer embedded in said first insulation layer, having a bottom in contact with the top face of said first conductive layer and a top face located on said second plane, and

a third conductive layer embedded in said second insulation layer, having a bottom in contact with the top face of said second conductive layer and a top face located on said third plane.

15. The semiconductor device according to claim 14, wherein said second conductive layer and said third conductive layer ~~are a~~ single layer formed continuously.

16. The semiconductor device according to claim 14, wherein

said first insulation layer and said second insulation layer are a single layer formed continuously, and

said second conductive layer and said third conductive layer are a single layer formed continuously.

17. The semiconductor device according to claim 14, wherein each of

said first and second insulation layers includes an SOG film into which impurities are introduced by ion implantation.

18. The semiconductor device according to claim 17, wherein each of said first and second insulation layers includes a silicon nitride film on said SOG film.

19. The semiconductor device according to claim 14, wherein said first conductive layer is embedded in a planarized insulation layer.

20. The semiconductor device according to claim 19, wherein said insulation layer includes an SOG film into which impurities are introduced by ion implantation.